Amendments to the Specification

On page 1, please amend paragraph 1 as follows:

The present invention is a continuation of pending U.S. Application Serial No. 10/016,183 entitled "Apparatus and Method for Determining Effect of On-Chip Noise on Signal Propagation" filed 30 October 2001 and assigned to the same assignee as the present invention.

On page 4, after paragraph 26, please insert the following new paragraph:

--FIG. 10 is a detailed view of operation 903 of the operational process illustrated in FIG. 9 according to one embodiment.--

On page 8, please amend paragraph 42 as follows:

The predicted operating frequency can be found by computer simulation of the circuit. Furthermore, the active operating frequency of TC24 is used to determine the effects of cross-talk on components within the core logic area. The active operating frequency ~~of~~ can also be found using computer simulation, but the effects on operating frequency caused by cross-talk and noise are generally not determined at this stage as most simulators do not account for these factors. It should be noted that the cross-talk analysis can be targeted to a specific layout topology or core logic component by routing the traces **50**, **52**, **54** of TC24 within a specific device layer or constraining the traces of TC24 to a specific routing methodology.

On page 11, please amend paragraph 56 as follows:

The testing system **86** is comprised of a testing apparatus **21**, a signal generator **88**, and a signal analyzer **90**, among others. In the current embodiment, the testing apparatus **21** is comprised of a plurality of ring oscillators. The ring oscillators are constructed such that they can dynamically measure the effects of noise and cross-talk on the memory device **80**, as discussed in conjunction with FIGS. 1 – 7C.

On page 12, please amend paragraph 59 as follows:

As previously mentioned the testing system **86** includes a signal generator **88**. The signal generator **88** in the current embodiment produces a 'clr' signal and a 'run' signal, among others. The 'clr' and 'run' signals are provided to each of the ring oscillators as discussed in conjunction with ~~FIG. 7~~ FIGS. 7A – 7B. The testing system **86** also includes a signal analyzer **90**. The signal analyzer **90** of the current embodiment retrieves the output signals (~~also~~ as discussed in conjunction with FIG. 7C) from the ring oscillators.

On page 13, please amend paragraph 65 as follows:

After the IC chip is deactivated, operation **903** begins to gather the test circuits' inactive information. In the current embodiment, operation **903** gathers the inactive information by sequentially activating and deactivating the four test circuits TC22, TC24, TC26, TC28 discussed above in conjunction with FIGS. 2 – 5. For example, as illustrated in FIG. 10, operation **903** activates TC22 (e.g., the first test circuit) and determines its inactive operating frequency (i.e., the operating reference signal). TC22 is then deactivated and TC24 (e.g., the second test circuit) is activated. The inactive operating frequency of TC24 is determined and TC24 is deactivated. Operation **903** then continues to activate and deactivate the remaining test circuits (here, TC26 [e.g., the third test circuit] and TC28 [e.g., the fourth test circuit]). Each test circuit is activated for the predetermined time period, T, as discussed above.

On page 26, amend the Abstract of the Disclosure as follows:

An integrated circuit testing apparatus having at least two of a ~~first~~ test circuit producing a signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within the integrated circuit; a ~~second~~ test circuit producing a signal for determining at least one of a cross-talk effect on the plurality of components and the accuracy of an interconnect capacitance extraction value; a ~~third~~ test circuit producing a signal for determining at least one of an effect of system noise on the operational speed of the plurality of components and a maximum degradation expected for a logic path between the plurality of components; and a ~~fourth~~ test circuit producing a signal for determining an effect of power supply noise on a signal propagation delay within the plurality of components.